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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/802,046	03/08/2001	Paul Strong	ARC.009A	2805

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GAZDZINSKI & ASSOCIATES
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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/802,046	STRONG ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-41 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) 1-41 are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-11, drawn to a method for preventing pipeline stalls on an instruction boundary using determining if instructions have merged, classified in class 712, subclass 210.

II. Claims 12-21, and 35, drawn to a system that inserts and processes a breakpoint instruction in an instruction sequence, classified in class 712, subclass 227.

III. Claims 22-23, drawn to a method for enhancing performance by simulating operation of processor and identifying a critical path within processing the program based on the act of simulating, classified in class 703, subclass 22.

IV. Claims 24-31, 36-37, drawn to processing an instruction using bypassing of data stored in a register, classified in class 712, subclass 218.

V. Claims 32-34, drawn to a system for operating a cache allowing instruction words to advance one stage ahead of the data word in the data cache, classified in class 711, subclass 215.

VI. Claims 38-41, drawn to a method for optimizing design of an integrated circuit, classified in class 703, subclass 21.

The inventions are distinct, each from the other because of the following reasons:

Inventions I, and II,III,IV,V,VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as a method for preventing pipeline stalls on an instruction boundary using determining if instructions have merged but did not insert and process a breakpoint instruction in an instruction sequence or identify a critical path within processing the program based on the act of simulating or process an instruction using bypassing of data stored in a register or operate a cache allowing instruction words to advance one stage ahead of the data word in the data cache or optimize design of an integrated circuit. See MPEP § 806.05(d).

Inventions II, and I,III,IV,V,VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention II has separate utility such as a system that inserts and processes a breakpoint instruction in an instruction sequence but did not prevent pipeline stalls on an instruction boundary using determining if instructions have merged or identify a critical path within processing the program based on the act of simulating or process an instruction using bypassing of data stored in a register or operate a cache allowing instruction words to advance one stage ahead of the data word in the data cache or optimize design of an integrated circuit. See MPEP § 806.05(d).

Inventions III, and I,II,IV,V,VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if

they are shown to be separately usable. In the instant case, invention III has separate utility such as a method for enhancing performance by simulating operation of processor and identifying a critical path within processing the program based on the act of simulating but did not prevent pipeline stalls on an instruction boundary using determining if instructions have merged or insert and process a breakpoint instruction in an instruction sequence or identify a critical path within processing the program based on the act of simulating or process an instruction using bypassing of data stored in a register or operate a cache allowing instruction words to advance one stage ahead of the data word in the data cache or optimize design of an integrated circuit. See MPEP § 806.05(d).

Inventions IV, and I,II,III,V,VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention IV has separate utility such as processing an instruction using bypassing of data stored in a register but did not prevent pipeline stalls on an instruction boundary using determining if instructions have merged or insert and process a breakpoint instruction in an instruction sequence or identifying a critical path within processing the program based on the act of simulating or operate a cache allowing instruction words to advance one stage ahead of the data word in the data cache or optimize design of an integrated circuit. See MPEP § 806.05(d).

Inventions V, and I,II,III,IV,VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if

they are shown to be separately usable. In the instant case, invention V has separate utility such as system for operating a cache allowing instruction words to advance one stage ahead of the data word in the data cache but did not prevent pipeline stalls on an instruction boundary using determining if instructions have merged and insert and process a breakpoint instruction in an instruction sequence or identify a critical path within processing the program based on the act of simulating or process an instruction using bypassing of data stored in a register or optimize design of an integrated circuit. See MPEP § 806.05(d).

Inventions VI, and I,II,III,IV,V are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention VI has separate utility such as method for optimizing design of an integrated circuit but did not prevent pipeline stalls on an instruction boundary using determining if instructions have merged or insert and process a breakpoint instruction in an instruction sequence or identify a critical path within processing the program based on the act of simulating or process an instruction using bypassing of data stored in a register or operate a cache allowing instruction words to advance one stage ahead of the data word in the data cache. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ERIC COLEMAN
PRIMARY EXAMINER